Your mom - outline

#### ****1. Introduction**** *(1 page)*

* Already expanded—done!
* You’ve got a strong motivation and overview of challenges already.

#### ****2. Background on LFSRs**** *(1–1.5 pages)*

* Detailed math on how serial LFSRs work.
* Finite field (GF(2)) operations and characteristic polynomials.
* Include diagrams of a serial LFSR and a state-transition matrix.

#### ****3. Limitations of Serial LFSRs**** *(0.5–1 page)*

* Throughput bottlenecks in serial designs.
* Clock cycle limitations per bit.
* Energy-per-bit and area constraints.
* Discuss fanout delay and feedback propagation.

#### ****4. Review of Parallel Architectures**** *(2 pages)*

* Matrix-based approaches (A, A², … Aⁿ precomputation).
* Feedback logic unrolling.
* Include figures of parallel LFSR block diagrams.
* Summary of existing literature with pros/cons table.

#### ****5. Proposed Design**** *(2–2.5 pages)*

* Architecture diagram with pipeline stages.
* Description of parallel matrix logic and how it’s implemented.
* Clock gating logic for power saving.
* Tradeoffs and constraints.
* State diagram or timing diagram.

#### ****6. Case Study: CRC-32 Parallel Generator**** *(1–1.5 pages)*

* Explain CRC use case and generator polynomial.
* Implementation and optimization for 32-bit LFSR.
* Discuss fan-in and fan-out challenges.

#### ****7. Simulation and Analysis**** *(1–1.5 pages)*

* Clock cycles vs serial implementation.
* Area comparison (estimated gates).
* Power analysis (activity factor, toggles).
* Throughput calculation in Mbps/Gbps.
* Add tables and graphs.

#### ****8. Discussion and Future Work**** *(1 page)*

* Reconfigurable LFSRs (switchable taps).
* FPGA-specific optimization ideas.
* Real-time random number generation use cases.

#### ****9. Conclusion**** *(0.5 page)*

* Summarize benefits and results.
* Reiterate relevance to modern hardware systems.

#### ****10. References**** *(1 page)*